more time consuming translation of this same information, as was typically done in the prior art.

As will be apparent to those skilled in the art, there are other specific circuits and structures beyond and/or in addition to those explicitly described herein which will serve to implement the translation mechanism of the present invention. Finally, although the above description enables the specific embodiment described herein, these specifics are not intended to restrict the invention, which should only be limited as defined by the following claims.

I claim:

1. A circuit for storing address translation information, said circuit comprising:
   a) a data path for receiving a virtual address, said virtual address including a segment identifier and a segment offset; and
   b) a segment descriptor memory coupled to said data path and selectable by said segment identifier, said memory capable of storing at least the following:
      I) linear address information describing the base of the segment,
      ii) linear address information describing the limit of the segment, and
      iii) a page frame describing at least a portion of a physical address of said segment.

2. The circuit of claim 1, wherein the segment descriptor memory is one or more registers.

3. The circuit of claim 1, wherein the segment descriptor memory is a cache.

4. The circuit of claim 1, further including a physical address register coupled to the segment descriptor memory for storing a physical address, said physical address

being comprised of the page frame from said segment descriptor memory and a page offset.

5. The circuit of claim 4, wherein the physical address stored in the physical address register is used to perform a memory access.

6. The circuit of claim 1, wherein the segment descriptor memory is further capable of storing:

(iv) information describing whether said page frame can be used for an address translation.

7. In a system having both a segmentation unit and a paging unit for translating physical addresses from virtual addresses, said virtual addresses including a segment identifier and segment offset, the improvement wherein:

the segmentation unit includes a segment descriptor memory selectable by said segment identifier, said memory capable of storing at least the following:

I) linear address information describing the base of the segment,

ii) linear address information describing the limit of the segment, and

iii) physical address information relating to said segment.

8. A circuit for storing address translation information in a computer system, said computer using both segmentation and paging to translate a virtual address having a segment identifier and segment offset into a physical address, said circuit comprising:

a segment descriptor memory selectable by said segment identifier, said memory capable of storing at least the following:

I) linear address information describing the base of the segment,

ii) linear address information describing the limit of the segment, and

iii) page frame describing at least a portion of a physical address of said segment.

9. An address translation system for translating a virtual address having a segment identifier and an offset field into a physical address, said address translation system being used in a computer system and comprising:

(a) a segmentation unit for generating linear address information based on the virtual address information, and for storing first physical address information having a first physical page frame and a first physical page offset;

(b) a paging unit coupled to the segmentation unit for generating said first physical page frame and second physical address information having a second physical page frame and a second page offset; and

© said segmentation unit further including:

[1] a segment descriptor memory, selectable by said segment identifier of said virtual address, and capable of storing

I) linear address information describing the base of the segment,

ii) linear address information describing the limit of the segment,

iii) said first physical page frame;

[2] a limit comparator for comparing whether the offset field exceeds the limit of the segment;

wherein a system memory access can be made by said computer system based on said first physical address information.

10. The system of claim 9, wherein the segmentation unit further includes a physical address comparator for comparing the first physical page frame and the second physical page frame, and wherein the memory access is canceled only if the first physical page frame and second physical page frame are not equal.

11. The system of claim 9, wherein the segmentation unit further includes an adder, and the first physical page offset can be generated by adding a portion of the virtual address offset field and a portion of the segment base in the segment descriptor memory.

12. The system of claim 9, wherein the first physical page offset can be generated by adding the virtual address offset field and the segment base in the segment descriptor memory.

13. The system of claim 9, wherein the paging unit further includes a page cache for storing page frames of physical pages most recently used by the computer system.

14. The system of claim 9, wherein the segment descriptor memory comprises one at least a register and/or cache.

15. The system of claim 9, wherein the first physical page frame generated by the paging unit is stored in the segment descriptor memory of the segmentation unit and can be used in a subsequent virtual to physical address translation.

16. The system of claim 9, wherein the segment descriptor memory is further capable of storing:

(iv) information describing whether said page frame can be used for an address translation.

17. The system of claim 9, wherein the segmentation unit also uses either or both index and displacement information to generate the linear address information.

18. A system for address translation in a CPU comprising:

a) an instruction set employing virtual addresses for accessing data or instructions located at physical addresses in a memory subsystem, said virtual addresses containing a segment identifier field selecting a segment and a segment offset field selecting an offset within the selected segment;

b) a segmentation circuit for generating linear addresses based on the virtual addresses, and for storing physical address information, said segmentation circuit including at least one segment descriptor memory selectable by said segment identifier, said segment descriptor memory capable of storing:

(I) segment data describing a segment, said segment data including linear address information describing the base and limit of the segment in a linear address space;

(ii) a physical address information corresponding to a page frame;

c) a paging circuit for receiving the linear addresses and generating physical addresses, said paging circuit including a page cache, said page cache optionally storing page frame and page offset field information for said CPU; and

d) a bus interface, capable of coupling the segmentation and paging circuits of the CPU to the memory subsystem, and for performing memory accesses in response to physical address information from either of said segmentation and paging circuits.

19. The circuit of claim 18, wherein the segment descriptor memory is one or more registers, or a cache.

20. The system of claim 18, wherein said bus interface provides either separate address/data lines to said memory, or multiplexed address/data lines.

21. The system of claim 18, wherein the segmentation circuit further includes a physical address comparator for comparing the page frame in the segmentation circuit descriptor memory with the page frame in the page cache, and wherein the

memory access is canceled only if the page frame in the segmentation circuit segment descriptor memory is different from the page frame in the page cache.

22. The system of claim 18, wherein the segmentation circuit further includes an adder, and a page offset is generated by adding a portion of the segment offset field to a portion of the segment base in the segment descriptor memory.

23. The system of claim 18, wherein the page frame generated by the paging unit is stored in the segmentation circuit.

24. The system of claim 18 wherein the segment descriptor cache is further capable of storing:

(iv) information describing whether said physical address information can be used for an address translation.

25. The system of claim 18, wherein the segmentation circuit uses index and/or displacement information to generate the linear addresses.

26. An address translation system for translating a virtual address having a segment and an offset field into a physical address, said address translation system being used in a computer system and comprising:

a) a segmentation unit for generating linear address information based on the virtual address information, and for generating and storing a physical address including a page frame and a page offset, said segmentation unit further including:

b) [1] a segment descriptor memory, selectable by said segment identifier of said virtual address, and capable of storing

I) linear address information describing the base of the segment,

ii) linear address information describing the limit of the segment,

iii) said page frame;

[2] a physical address memory for storing said physical address including said page frame number and a page offset; and

wherein an access to a memory subsystem can be made by said computer system based on said physical address.

27. The system of claim 26, wherein the segmentation unit further includes a physical address comparator for comparing the page frame from said virtual address with a page frame corresponding to a different, later in time virtual address, and wherein the memory access is canceled only if the page frames of said different virtual addresses are not equal.

28. The system of claim 26, wherein the segmentation unit further includes an adder, and the page offset is generated by adding a portion of the virtual address offset field and a portion of the segment base in the segment descriptor memory, and then stored in a register corresponding to the first physical address memory.

29. The system of claim 26, wherein the segment descriptor memory includes at least a register and/or a cache.

30. The system of claim 26, further including a bus interface capable of coupling the segmentation unit to the memory subsystem, and for performing memory accesses in response to physical address information from said segmentation unit.

31. The system of claim 30, wherein said bus interface provides either separate address/data lines to said memory, or multiplexed address/data lines.

32. The system of claim 26, wherein the segment descriptor memory is further capable of storing:

(iv) information describing whether said page frame can be used for an address translation.

33. The system of claim 26, wherein the segmentation unit also uses either or both index and displacement information to generate the linear address information.

34. A method of calculating physical addresses from virtual addresses, said method comprising:

a) calculating a first physical address, having a first page frame field and a first page offset field, based on a virtual address;

b) storing said first page frame field of said first physical address;

c) calculating a second physical address based on a second virtual address including a second page frame field and a second page offset field;

d) generating a third physical address based on the first page frame field and the second page offset field;

e) generating a memory access request based on said third physical address.

35. The method of claim 34, further including a step: (f) canceling said access request to memory using said third physical address if the first page frame field is not equal to the second page frame field of said second physical address.

36. The method of claim 34, wherein the page frame fields most recently used by the computer system are stored.

37. The method of claim 34, further including a step: checking whether the first page frame field can be used for an address translation.